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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,467	02/26/2004	Kristopher Craig Whitney	ROC920030309US1	7026

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,467	WHITNEY, KRISTOPHER CRAIG	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on September 07, 2006 for the application of Whitney, for a "Method for achieving higher availability of computer PCI adapters" filed February 26, 2004.

Claims 1-18 are pending in the application.

Claims 1, 4, 7-8, 11, 18 are rejected under 35 USC § 102.

Claims 2-3, 5-6, 9-10, 12-17 are rejected under 35 USC § 103.

Claims 1, 4, and 12, have been amended.

Claim 18 has been added.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 7-8, 11, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Emerson et al. (U.S. Patent No. 6,173,341).

As per claim 1, Emerson discloses a computer system comprising:

a system processor (Fig. 2, element 102)

an input/output processor (Fig. 2, element 210)

an input/output adaptor (Fig. 2, element 114) connected to the system processor and the input/output processor, and configured to be dynamically switchable between

being controlled by the system processor and being controlled by the input/output processor (col. 8, lines 40-54).

As per claim 4, Emerson discloses a method for fault recovery in a computer system having a system processor (Fig. 2, element 102), an input/output processor (Fig. 2, element 210), and an input/output adaptor (Fig. 2, element 114) connected to the system processor and the input/output processor (Fig. 2) the input/output adaptor being configured to be dynamically switchable between being controlled by the system processor and being controlled by the input/output processor (col. 8, lines 30-54) the method for fault recovery comprising:

detecting a fault in the input/output processor and switching the input/output adapter to control by the system processor if the input/output adapter is being controlled by the input/output processor when the fault is detected (col. 8, lines 30-54).

As per claim 7, Emerson discloses the computer system has a plurality of dynamically switchable input/output adapters (Fig. 2, element 114) and each of the dynamically switchable input/output adapters being controlled by the input/output processor (Fig. 2, element 210) when the fault is detected is switched to control by the system processor (col. 8, lines 30-54).

As per claim 8, Emerson discloses detecting correction of the fault in the input/output processor (Fig. 2, element 210) switching the input/output adapter to

control by the input/output processor when the correction of the default is detected, if it was previously switched to control by the system processor as a result of the fault in the input/output processor (col. 8, lines 30-54).

As per claim 11, Emerson discloses the computer system has a plurality of dynamically switchable input/output adapters (Fig. 2, element 114) and each of the dynamically switchable input/output adapters being controlled by the system processor (Fig. 2, element 102) when the correction of the fault is detected is switched to control by the input/output processor if it was previously switched to control by the system processor as a result of the fault in the input/output processor (col. 8, lines 30-54).

As per claim 18, Emerson discloses a computer system according to claim 1, wherein the input/output adapter, the input/output processor and the system processor are interconnected via a bus (Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2-3, 5-6, 9-10, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson et al. (U.S. Patent No. 6,173,341) in view of Odenwald et al. (U.S. Patent No. 6,223,240).

As per claims 2, 5, 9, and 16 Emerson fails to explicitly disclose a PCI adaptor.

Odenwald teaches:

the input/output adapter is a PCI (Peripheral Component Interconnect) adapter (Fig. 2).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of configuring adapters in a computer system of Emerson et al.'s in combination with the method of sharing processing load among a plurality of devices of Odenwald et al.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Emerson et al. discloses a method of assigning input/output adapters to input/output processors and host system processors

(Figs. 2 and 4). Odenwald et al. discloses a method of using a bus bridge to connect input/output adapters and processors to the host processor to provide an improved method for input/output transaction processing (col. 9, lines 9-20).

As per claim 3, 6, 10, and 17 Emerson fails to explicitly disclose a PCI compatible processor.

Odenwald teaches:

the input/output processor is a PCI-compatible processor (Fig. 2).

As per claim 12, Emerson discloses input/output adaptor being configured to be dynamically switchable between being controlled by the system processor and being controlled by the input/output processor (col. 8, lines 40-54).

Emerson fails to explicitly disclose a method for optimizing processor utilization.

Odenwald teaches:

a method for optimizing processor utilization in a computer system having a system processor (Fig. 7, element 702), an input/output processor (Fig. 7, element 718), and an input/output adaptor (Fig. 7, element 720) connected to the system processor and the input/output processor (Fig. 7), the method for optimizing utilization comprising:

determining computer system utilization and switching control of the input/output adapter from a first one of the system processor and the input/output processor to a second one of the system processor and the input/output processor, if it is determined that the first one of the processors is being over utilized and that the second one of the

processors has sufficient capacity that switching control of the input/output adapter will not adversely affect system throughput (col. 8, lines 2-15).

As per claim 13, Emerson fails to explicitly disclose a method for optimizing processor utilization.

Odenwald teaches:

switching control of the input/output adapter from the first one of the processors to the second one of the processors is further based on a determination that the over utilization of the first of the processors is likely to continue for at least a specified period of time (col. 8, lines 2-15).

As per claim 14, Emerson fails to explicitly disclose a method for optimizing processor utilization.

Odenwald teaches:

the steps of determining computer system utilization switching control of the input/output adapter based on such determination are repeated at intervals substantially equal to the specified period of time (col. 8, lines 2-15).

As per claim 15, Emerson fails to explicitly disclose a method for optimizing processor utilization.

Odenwald teaches:

the computer system has a plurality of dynamically switchable input/output adapters (Fig. 7), and the steps of determining computer system utilization switching control of the input/output adapter based on such determination are performed for each of the plurality of input/output adapters (col. 8, lines 2-15).

Response to Arguments

Applicant's arguments have been fully considered with the examiner's response detailed below.

Applicant's arguments see pages 7-13, filed September 07, 2006 with respect to the rejection(s) of claim(s) 1-18 under 35 USC § 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made over Emerson et al. (U.S. Patent No. 6,173,341) in view of Odenwald et al. (U.S. Patent No. 6,223,240). Refer to the corresponding section of the claim analysis for details.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).